AD-A191 509 PLANAR FULLY ION-IMPLANTED HIGH POWER INP MISFETS(U) 1/1
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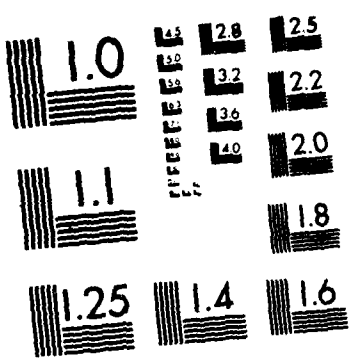

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T DOCUMENTATION PAGE

1a	1b. RESTRICTIVE MARKINGS
2a AD-A191 589	3. DISTRIBUTION/AVAILABILITY OF REPORT
2b.	Approved for public release; distribution is unlimited.
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: Naval Ocean Systems Center	6b. OFFICE SYMBOL (If applicable): NOSC
7a. NAME OF MONITORING ORGANIZATION: Naval Ocean Systems Center	
6c. ADDRESS (City, State and ZIP Code): San Diego, California 92152-5000	7b. ADDRESS (City, State and ZIP Code): San Diego, California 92152-5000
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Naval Research Laboratory	8b. OFFICE SYMBOL (If applicable): NRL
9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER	
8c. ADDRESS (City, State and ZIP Code): 4555 Overlook Avenue, Washington, DC 20375	10. SOURCE OF FUNDING NUMBERS

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	AGENCY ACCESSION NO.
62762N	EE90	XF62588	DN488 778

11. TITLE (Include Security Classification)
Planar Fully Ion-Implanted High Power InP MISFETs

12. PERSONAL AUTHOR(S)
L.J. Messick, R. Nguyen, and D.A. Collins

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Professional paper	FROM Aug 1987 TO Aug 1987	December 1987	

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	ion-implanted InP FET GaAs

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Planar fully ion-implanted InP power MISFETs using SiO_2 as the gate insulator have been fabricated. At 9.7 GHz CW with 3.7 dB gain 800 μm gate width devices exhibited power per unit gate width as high as 2.9 W/mm, more than twice the highest value ever reported for GaAs FETs. For comparison at the same CW frequency and 4 dB gain our 1 mm gate width mesa-type epitaxial InP power MISFETs have demonstrated power per unit gate width as high as 4.5 W/mm, more than three times the highest GaAs value.

Published in Proceedings of 1987 IEEE/Cornell Conference.

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20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL
L.J. Messick	619-553-1035	Code 561

DD FORM 1473, 84 JAN — 83 APR EDITION MAY BE USED UNTIL EXHAUSTED ALL OTHER EDITIONS ARE OBSOLETE

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PLANAR FULLY ION-IMPLANTED HIGH POWER InP MISFETs

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ABSTRACT

Planar fully ion-implanted InP power MISFETs using SiO_2 as the gate insulator have been fabricated. At 9.7 GHz CW with 3.7 dB gain 800 μm gate width devices exhibited power per unit gate width as high as 2.9 W/mm, more than twice the highest value ever reported for GaAs FETs. For comparison at the same CW frequency and 4 dB gain our 1 mm gate width mesa-type epitaxial InP power MISFETs have demonstrated power per unit gate width as high as 4.5 W/mm, more than three times the highest GaAs value.

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INTRODUCTION

In the case of GaAs MESFETs, low input impedance which decreases with the increasing gate width required for the achievement of high output power leads to difficulties in device utilization in microwave systems and places a limit on the useful power achievable with these devices. For this reason a different device or material with a capability for higher power output per unit gate width (power density) could considerably advance the technology of power amplification in the microwave and millimeter wave spectral regions [1, 2].

InP is an attractive material for high-frequency power FETs [1-6] because of its higher peak electron drift velocity, thermal conductivity and breakdown field [2] as compared to GaAs. However, InP MESFETs [5], because of the high leakage current of their Schottky gates, exhibited source-drain breakdown voltages much lower than expected and power densities disappointingly comparable to that of GaAs MESFETs. InP JFETs [6] exhibited similar power densities.

The metal-insulator-semiconductor field-effect transistor (MISFET) is an attractive device for power applications because of both its lower gate leakage current and the wider range of voltage which can be applied to its insulated gate as compared to the MESFET and the JFET. Mesa type InP MISFETs fabricated on epitaxial layers and having gate widths of 1 mm reported by us [1] and 300 μm reported by Armand et al. [2], have demonstrated power output per unit gate width as high as 4.5 W/mm which is over three times the highest value ever reported for GaAs FETs [7]. This paper reports results on the first high-power planar ion-implanted InP MISFETs.

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POWER MISFET FABRICATION

Figure 1 illustrates a schematic cross-section of the device, an n-channel depletion-mode structure fabricated by implanting directly into a substrate of Fe-doped semi-insulating InP with a resistivity of $\sim 10^7$ ohm-cm.

Contact regions selectively receive a multiple energy n^+ implant of Silicons using energies ranging from 40 to 360 keV and doses in the range 3 X 10^{13} cm^{-2} to 6 X 10^{14} cm^{-2}. The implant schedule is intended to produce a high-density, relatively flat carrier profile from close to the surface to a depth of at least approximately 0.4 μm. High carrier density near the surface may be particularly important for optimum ohmic contact formation. The precise schedule used is listed in figure 2 which illustrates the implanted impurity density versus depth (assuming Gaussian distributions with their first two moments predicted using Lindhard, Scharff, Schiot (LSS) theory) resulting from each individual energy implant as well as the total predicted density. Also shown in this figure are the results of an electrochemical carrier density profile measurement made using a Polaron profiler on an Fe-doped semi-insulating InP test sample which had been implanted with the specified schedule and subsequently activated.

The channel region selectively receives a multiple energy n-type implant of Si which overlaps the n^+ contact implanted regions for electrical continuity. Channel implant energies range between 60 and 360 keV with doses between 1X10^{12} cm^{-2} and 1.5X10^{13} cm^{-2}. In this case the schedule is intended to produce a carrier density in the low 10^{17} cm^{-3} range with as flat as possible a carrier profile from fairly close to the surface to about 0.4 μm falling off as abruptly as possible beyond that depth. Carrier density very near the surface is not critical in the channel region since, under the gate, approximately the first 0.2 μm of material is removed in the channel recessing fabrication step. A typical channel implant schedule, the corresponding predicted Si densities versus depth and measured resulting carrier density in an activated test sample versus depth are shown in figure 3. After implantation the wafers are capped with approximately 2000 Å of SiO_2 and subsequently annealed in forming gas at 725°C for 60 seconds to electrically activate the implant. This activation recipe produced activations of ~80% and mobilities of ~2000 cm^2 $V^{-1}sec^{-1}$ in Fe-doped InP test wafers which had received 50 keV Si implant doses of 5X10^{12} cm^{-2}.

After formation of alloyed AuGe ohmic contacts and definition of evaporated Au contact pads the device channels are chemically recessed using a solution of 10% HIO_3 in water; the deeply recessed structure being important for high-voltage high-power device operation [1, 2].

Next the SiO_2 gate insulator is deposited about 1000 Å thick by indirect-plasma-assisted CVD [8] at a temperature of about 3000°C using a gas mixture of SiH_4, O_2 and as a carrier gas N_2. Evaporated Al gates 0.5 μm thick are then defined by liftoff and finally bonding windows are opened in the SiO_2. The gate length is approximately 1 μm and the source drain spacing 5 μm. Figure 4 illustrates the device geometry.

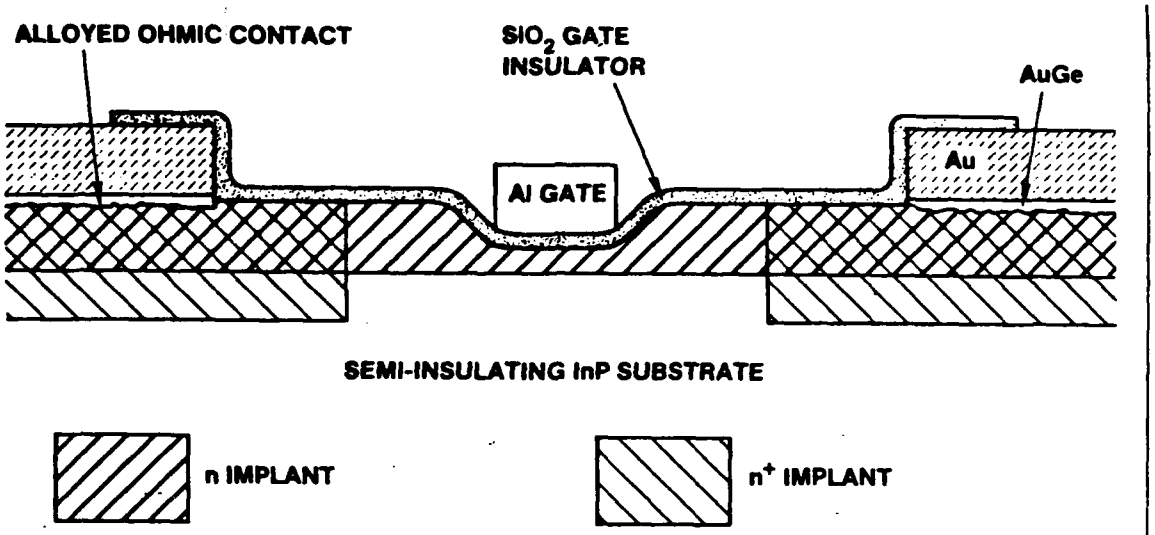


Figure 1. Planar fully implanted InP power MISFET schematic cross-section.

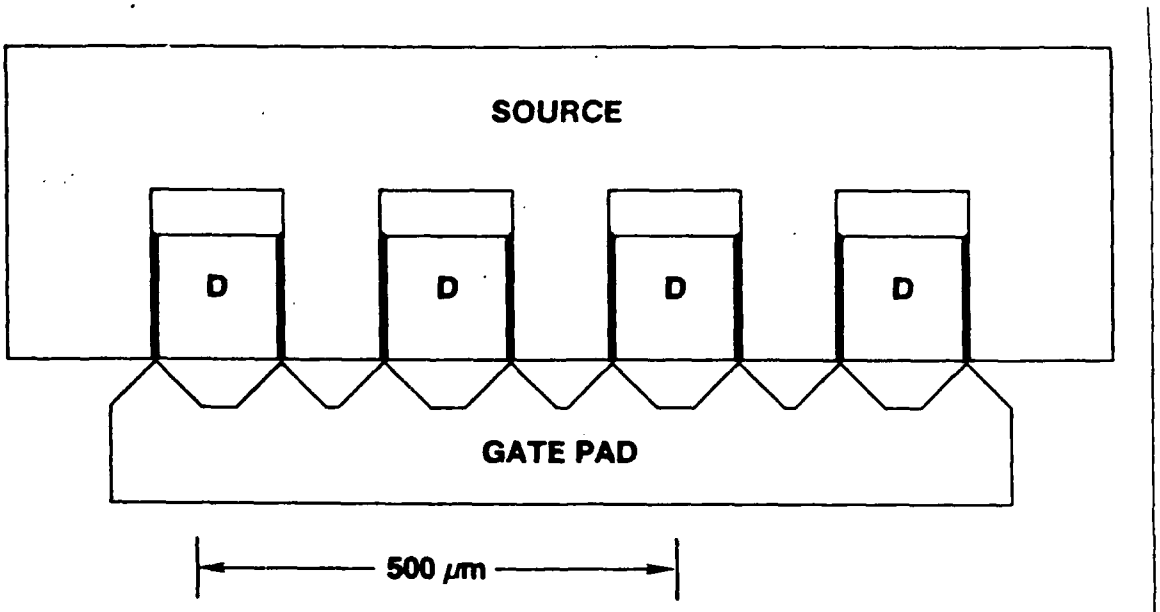
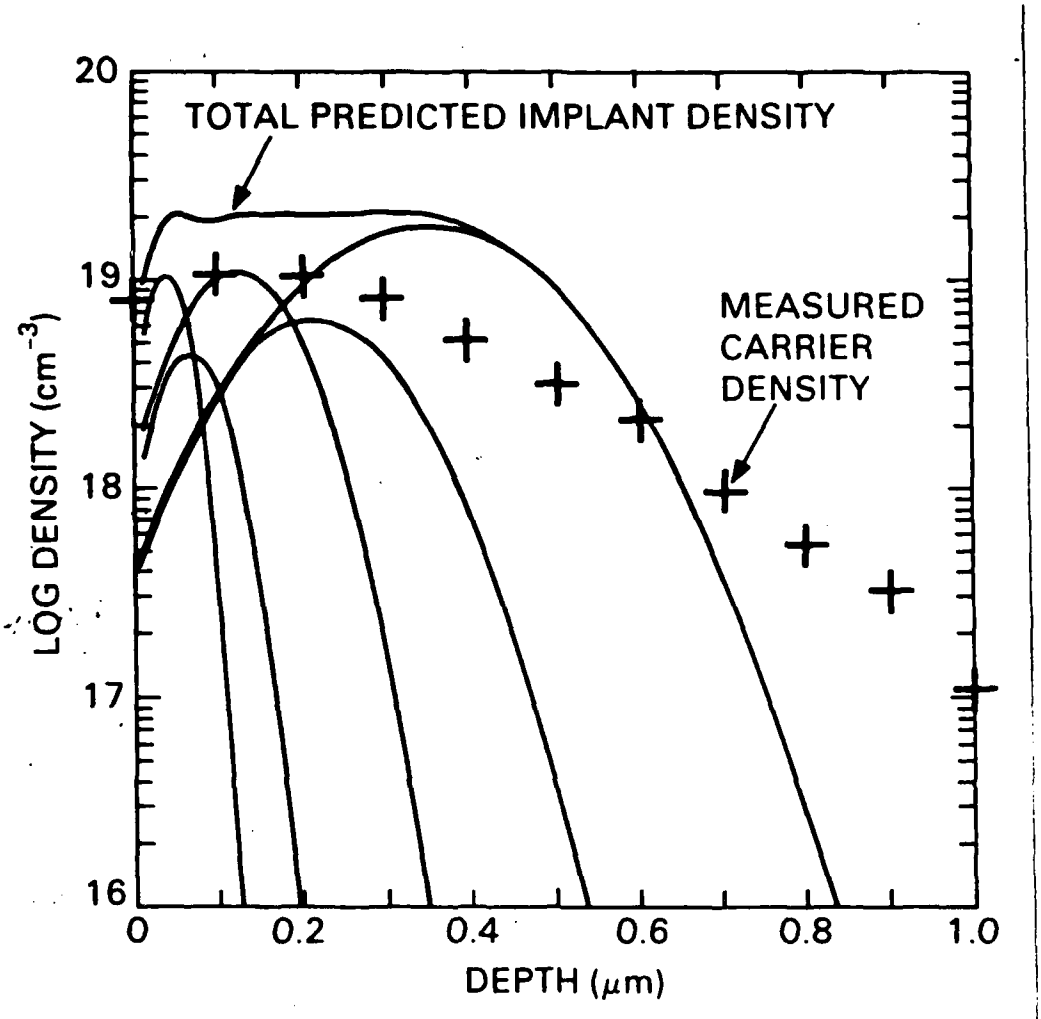
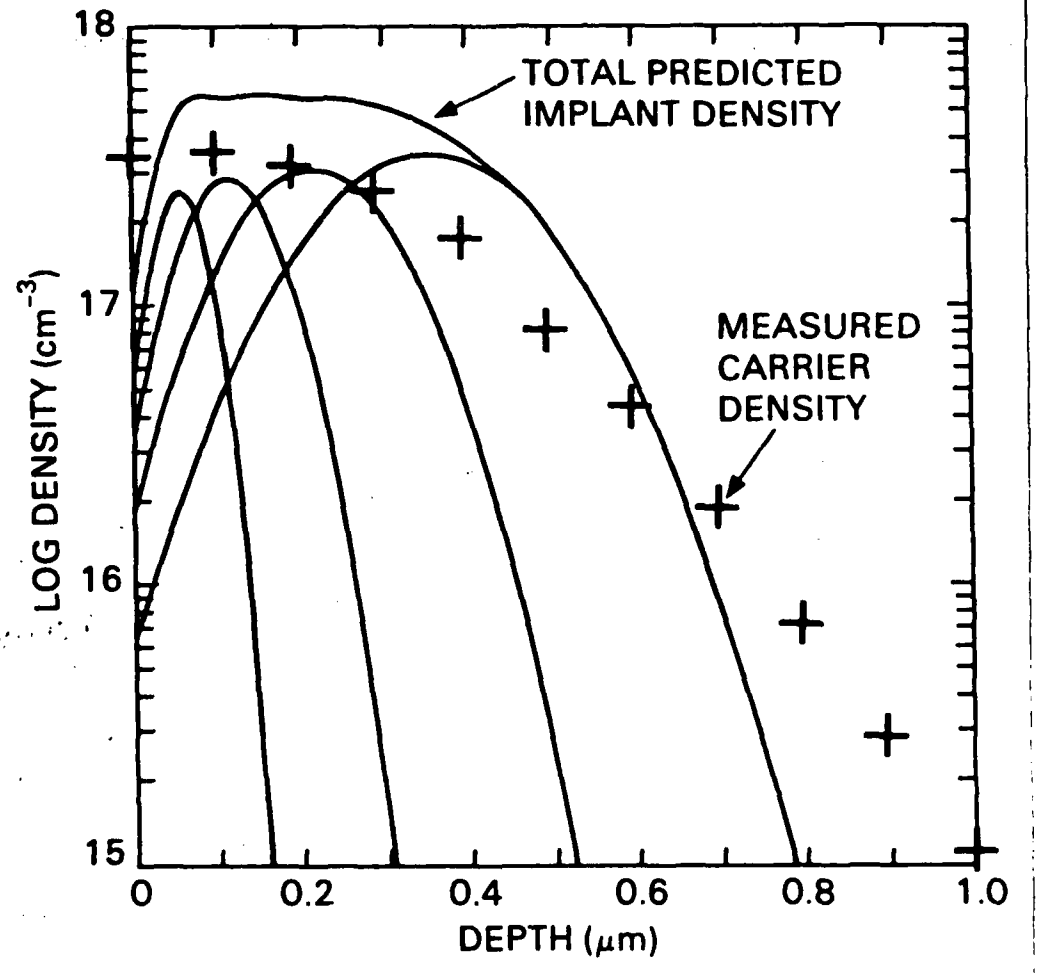


Figure 4. Fully implanted 1 mm gate width InP power MISFET geometry. For clarity only the contact n^+ implant and gate metallization regions are shown. Areas marked D are isolated drain regions requiring individual wire bonds. 0.8 mm gate widths were also used.



Energy (KeV)	Dose(cm^{-2})	Range(μm)	Std. Dev.(μm)
360	5.6E14	0.355	0.126
220	1.4E14	0.215	0.091
130	1.7E14	0.125	0.061
70	3.9E13	0.067	0.037
40	6.0E13	0.038	0.024

Figure 2. Contact n^+ Si implant data, predicted impurity densities vs. depth for each individual energy implant, total predicted impurity density and carrier density measured on a test sample.



Energy(keV)	Dose(cm^{-2})	Range(μm)	Std. Dev.(μm)
360	1.1E13	0.355	0.126
220	7.0E12	0.215	0.091
120	4.0E12	0.115	0.057
60	2.0E12	0.056	0.032

Figure 3. Typical channel n-type Si implant data, predicted impurity densities vs. depth for each individual energy implant, total predicted impurity density and carrier density measured on test sample.

RESULTS

Figure 5 shows a curve tracer photograph of the drain characteristics of a representative 1 mm wide device with a saturation drain current of around 580 mA per mm of gate width. The gate voltage is applied in 80 μs pulses.

Table I compares CW performance data for planar implanted InP MISFETs, our previous mesa-type epitaxial InP MISFETs [1] and the best ever reported GaAs FETs [7]. The highest power per unit gate width at approximately 4 dB gain for the implanted InP devices is 2.9 W/mm, over twice the highest value ever reported for GaAs FETs. This impressive number is still not quite as good as the value for the epitaxial InP devices of 4.5 W/mm, over three times the best GaAs value.

	Implanted InP MISFET	Epitaxial InP MISFET	Best GaAs MESFET
Frequency	9.7 GHz	9.7 GHz	8 GHz
Gate Width	0.80 mm	1.0 mm	1.2 mm
V_{DS} (At Maximum Power Output)	16.3 V	18 V	18 V
V_{GS} (At Maximum Power Output)	-3.0 V	0 V	
I_{DS} (At Maximum Power Output)	269 mA	327 mA	152 mA
Power Output (4 dB Gain)	2.34 W*	4.5 W	1.7 W
Power-Added Efficiency	31%	46%	37%
I_{DS}/Gate Width	336 mA/mm	327 mA/mm	127 mA/mm
Power Output/Gate Width	2.9 W/mm	4.5 W/mm	1.4 W/mm

*3.7 dB Gain

Table I. Power FET technology comparison.

As was first pointed out for epitaxial devices by Armand et al. [2] the high power densities of both the InP structures are largely due to their high drain bias current densities, in this case around 330 mA/mm as compared to 127 mA/mm for GaAs [7]. This high current density arises from the high peak electron drift velocity in InP as well as from the high product of channel thickness and carrier density in these devices. For both implanted and epitaxial InP MISFETs optimum values of gate bias voltage varied widely between devices while its effect on device performance was relatively small.

While differences in drain bias voltage and current per unit gate width between the best implanted and best epitaxial InP devices are relatively slight the lower power densities of the implanted devices are accompanied by lower power-added efficiencies in approximately the same ratio. This inferior performance of implanted devices compared to epitaxial devices might be due at least in part to the transition between the semi-insulating substrate and the channel being inherently less abrupt in implanted structures than in epitaxial ones. Because of this at least part of the channel has a lower than ideal doping density. Another partial cause might be the presence of Fe in device channels formed by implantation directly into the Fe-doped substrate. Even assuming these disadvantages persist however, these planar fully implanted devices might still be technologically important because of the greater ease, economy and reproducibility with which devices not requiring an epitaxial growth process can be fabricated and monolithically integrated with other devices.

Figure 6 illustrates at 9.7 GHz CW for the same implanted InP device referred to in Table I the dependence of power output, power-added efficiency and power gain on drain bias voltage with an RF input power of 1.25 W per mm of gate width.

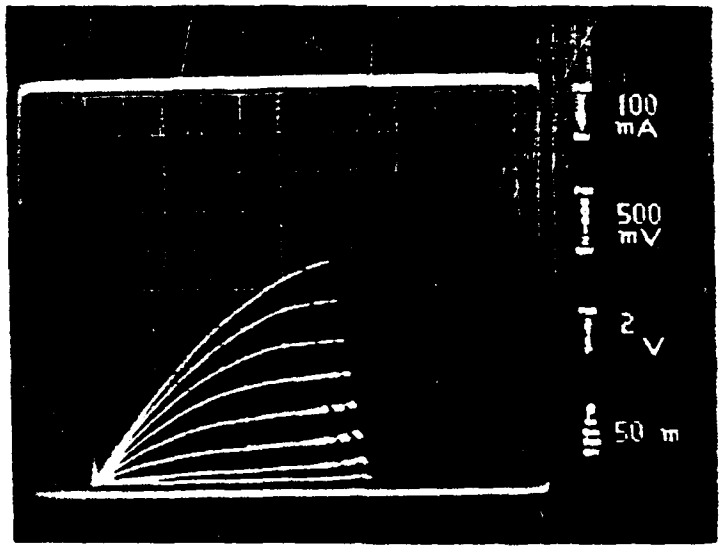


Figure 5. Drain characteristics of representative 1 mm wide implanted InP depletion-mode MISFET. 100 mA per major vertical division, 500 mv per major horizontal division, 2 V per step

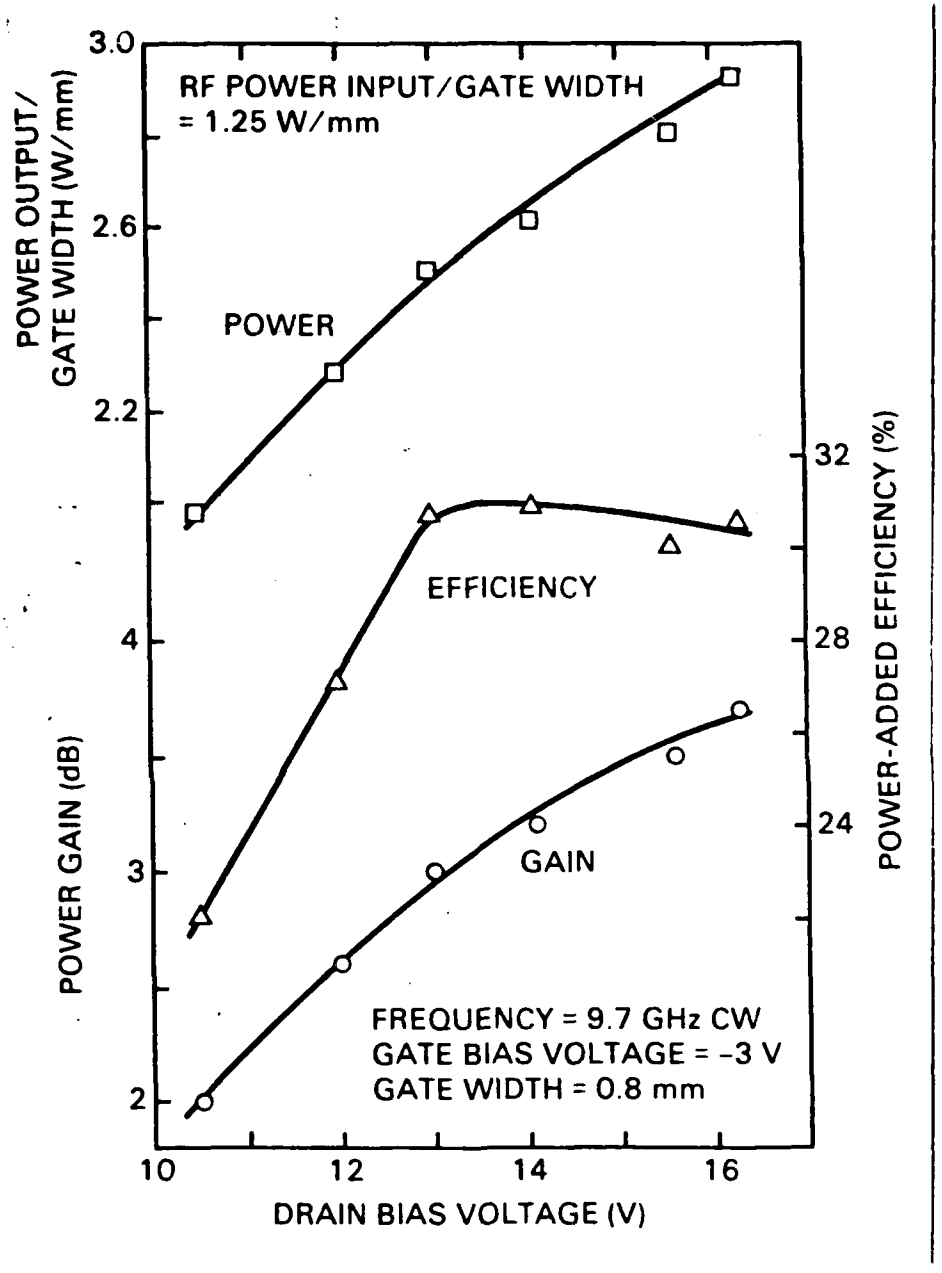


Figure 6. Power output, power-added efficiency and power gain vs drain bias voltage for an ion-implanted InP power MISFET

As has been discussed previously in regard to similar epitaxial devices [1, 2] for fixed gate and drain bias voltage the drain bias current of implanted InP power MISFETs decreases similarly with the magnitude of the RF input power. This effect appears to be due to the influence of the RF voltage applied to the MIS gate on the charge status of states residing in the neighborhood of the semiconductor/gate-insulator interface giving rise to an average channel depletion depth which increases with increasing RF input power. Consequently when these devices are operated at high drain bias voltage with no average current limit on the bias supply a large reduction in the RF power input will increase the drain bias current as well as reduce the amount of dc power converted to RF. The device will then have more dc power to disipate and thermal breakdown will result. For this reason safe operation at high drain bias voltage requires either that the RF input be maintained at a high level [1, 2] or that the average drain current be limited. This effect however, would present no problem for certain applications, for instance applications which don't necessarily require dc power to the device while the RF input is shut off, for example certain radar applications which only require pulses of constant RF power.

A stability test was performed on a 0.8 mm gate width implanted device with its gate and drain bias voltages held constant and its RF power input held at 1.25 W per mm of gate width. Power output was monitored as a function of time with the device operating continuously and with elapsed time equaling zero when bias and RF were first applied. Initially the power output was 2.6 W/mm at 3.2 dB gain. Over a period of 4 days the power fell by 14%. For comparison, mesa epitaxial InP power MISFETs [1] exhibited power output stable to within 2% over a week of continuous operation at an output level of 1.5 W/mm at 3 dB gain.

CONCLUSION

At 9.7 GHz CW and approximately 4 dB gain the power output per unit gatewidth of planar implanted InP power MISFETs is over twice the highest value ever reported for GaAs FETs [7] while that of mesa epitaxial InP power MISFETs is over three times the highest GaAs value.

InP power MISFETs promise substantial advances over GaAs FETs in high frequency power amplification.

ACKNOWLEDGEMENTS

The authors thank C. R. Zeisse, E. R. Schumacher and M. J. Taylor of the Naval Ocean Systems Center for their InP work on implantation, rapid annealing and characterization which helped make this work possible. We also thank N. T. Linh, M. Armand, and J. Chevrier of Thomson-CSF, H. M. Macksey of Texas Instruments and D. Rubin and A. K. Nedoluha of the Naval Ocean Systems Center for numerous productive discussions. This work was supported by the Naval Research Laboratory.

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